CLAIMS:

What we claim as our invention is:

1. A processor configured to execute an instruction comprising a user-defined value, wherein the user-defined value is either an address or a command, and to provide the user-defined value during execution of the instruction.

2. The processor as recited in claim 1, wherein the user-defined value comprises a plurality of ordered bits, and wherein values of the bits are assigned by a user.

3. The processor as recited in claim 1, wherein the processor comprises a bus interface adapted for coupling to a bus having a plurality of signal lines, and wherein the processor is configured to drive the user-defined value upon at least one signal line of the bus during execution of the instruction.

4. The processor as recited in claim 1, wherein the user-defined value is an address of an addressable register.

5. The processor as recited in claim 4, wherein the addressable register is accessed in response to the user-defined value.

6. The processor as recited in claim 1, wherein the processor is configured to provide the user-defined value, data corresponding to the user-defined value, and an asserted write control signal during execution of the instruction, and wherein the data is stored in the addressable register in response to the user-defined value, the data corresponding to the user-defined value, and the asserted write control signal.

7. The processor as recited in claim 1, wherein the user-defined value is a command having a corresponding predetermined function.

8. The processor as recited in claim 7, wherein the predetermined function corresponding to the command is performed in response to the user-defined value.

9. The processor as recited in claim 7, wherein the predetermined function produces a result, and wherein the processor is configured to receive the result.

10. The processor as recited in claim 9, wherein the processor is configured to provide the user-defined value and data corresponding to the user-defined value during execution of the instruction, and wherein the predetermined function uses the data to produce the result.

11. The processor as recited in claim 9, wherein the result is generated during execution of the instruction.

12. The processor as recited in claim 9, wherein the processor is configured to receive the result during execution of the instruction.

13. The processor as recited in claim 12, wherein the processor is configured to execute the instruction via a plurality of pipeline stages performed in sequence, and wherein the processor is configured to provide the user-defined value during a first one of the pipeline stages.

14. The processor as recited in claim 13, wherein the processor is configured to receive the result during a second one of the pipeline stages.

15. A processor, comprising:

a bus interface adapted for coupling to a bus having a plurality of signal lines; and

wherein the processor is configured to execute an instruction comprising a user-defined address, and to drive the user-defined address upon at least one signal line of the bus via the bus interface during execution of the instruction.

16. The processor as recited in claim 15, wherein the user-defined address comprises a plurality of ordered bits, and wherein values of the bits are assigned by a user.

17. The processor as recited in claim 15, wherein the user-defined address is an address of an addressable register.

18. The processor as recited in claim 17, wherein the addressable register is accessed in response to the user-defined address.

19. The processor as recited in claim 15, wherein the processor is configured to provide the user-defined address, data corresponding to the user-defined address, and an asserted write control signal during execution of the instruction, and wherein the data is stored in the addressable register in response to the user-defined address, the data corresponding to the user-defined value, and the asserted write control signal.

20. A data processing system, comprising:

a processor configured to execute an instruction comprising a user-defined address and to provide the user-defined address during execution of the instruction; and

a device comprising an addressable register, wherein the device is coupled to receive the user-defined address and configured to access the addressable register in response to the user-defined address.

21. The data processing system as recited in claim 20, wherein the device comprises a peripheral device, and wherein the peripheral device comprises the addressable register.

22. The data processing system as recited in claim 21, wherein the peripheral device comprises a timer, a serial port, or a parallel port.

23. The data processing system as recited in claim 21, wherein the addressable register is a control register, a status register, or a data register.

24. The data processing system as recited in claim 21, wherein the device comprises a data management unit coupled between the peripheral device and the processor and configured to receive read data from the peripheral device and to provide the read data to the processor.

25 24. The data processing system as recited in claim 21, wherein the peripheral device is configured to produce a first interrupt signal when in need of service, and wherein the device comprises an interrupt control unit coupled between the peripheral device and the processor and configured to receive the first interrupt signal from the peripheral device and to provide a second interrupt signal to the processor in response to the first interrupt signal.

26 25. The data processing system as recited in claim 24, wherein the first interrupt signal has a corresponding priority, and wherein the second interrupt signal comprises a value specifying the priority.

27 26. The data processing system as recited in claim 24, wherein the processor comprises a plurality of registers and logic for controlling the registers, wherein the logic is configured to operate the registers in response to the second interrupt signal such that in the event an interrupt request having a higher priority than an interrupt request currently being handled is received, an interrupt service routine of the interrupt request having the higher priority is completed before an interrupt service routine of the interrupt request currently being handled.

28 27. The data processing system as recited in claim 20, wherein the processor is configured to execute the instruction via an execution pipeline comprising a plurality of pipeline stages performed in sequence.

29 28. The data processing system as recited in claim 27, wherein in the event the instruction specifies a read operation, the processor is configured to provide the user-defined address and an asserted read control signal during a first one of the pipeline stages, and to receive read data obtained from the addressable register during a second one of the pipeline stages.

30 29. The data processing system as recited in claim 28, wherein the processor comprises a bus interface adapted for coupling to a bus having a plurality of signal lines, and wherein the processor is configured to drive the user-defined address and the asserted read control signal upon signal lines of the bus during the first one of the pipeline stages.

31 30. The data processing system as recited in claim 29, wherein the bus interface comprises stall logic adapted to receive a ready signal from the device and configured to assert a stall signal in the event the ready signal is not asserted during the second one of the pipeline stages, and wherein in response to the stall signal the execution pipeline is stalled.

32 31. The data processing system as recited in claim 27, wherein in the event the instruction specifies a read-modify-write operation, the processor is configured to provide the user-defined address, an asserted read control signal, and an asserted write control signal during a first one of the pipeline stages, to receive data obtained from the addressable register as read data during a second one of the pipeline stages, to modify the data during a third one of the pipeline stages, and to provide the modified data as write data during a fourth one of the pipeline stages.

33 32. The data processing system as recited in claim 31, wherein the processor comprises a bus interface adapted for coupling to a bus having a plurality of signal lines, and wherein the processor is configured to drive the user-defined address, the asserted read control signal, and the asserted write control signal upon signal lines of the bus during the first one of the pipeline stages, to receive the read data during the second one of the pipeline stages, and to drive the write data upon signal lines of the bus during the fourth one of the pipeline stages.

34 33. The data processing system as recited in claim 32, wherein the bus interface comprises a bit manipulation unit coupled to receive the read data as input, to modify the data, and to produce the modified data.

35 34. A method for obtaining a value stored in an addressable register, comprising:

driving an address of the addressable register on a plurality of address signal lines of a bus, and an asserted read control signal on a read control signal line of the bus, during a first stage of an instruction execution pipeline; and

receiving the value via a plurality of data signal lines of the bus when a corresponding ready signal driven on a ready signal line of the bus is asserted during a second stage of the instruction execution pipeline subsequent to the first stage.

36 35. The method as recited in claim 34 wherein a time period between the first and second stages of the instruction execution pipeline is extended in the event of a stall condition.

37 36. A method for providing a value stored in an addressable register, comprising:

receiving an address driven on a plurality of address signal lines of a bus when a read control signal driven on a read control signal line of the bus is asserted during a first stage of an instruction execution pipeline; and

if the address is an address of the addressable register, driving the contents of the addressable register on a plurality of data signal lines of the bus, and an asserted ready signal on a ready signal line of the bus, during a second stage of the instruction execution pipeline subsequent to the first stage.

38 37. A method for storing a value in an addressable register, comprising:

driving an address of the addressable register on a plurality of address signal lines of a bus, and an asserted write control signal on a write control signal line of the bus, during a first stage of an instruction execution pipeline; and

driving the value to be stored in the addressable register on a plurality of data signal lines of the bus, and an asserted ready signal on a ready signal line of the bus, during a second stage of the instruction execution pipeline subsequent to the first stage.

39 38. The method as recited in claim 37 wherein a time period between the first and second stages of the instruction execution pipeline is extended in the event of a stall condition.

40 39. A method for storing a value in an addressable register, comprising:

receiving an address driven on a plurality of address signal lines of a bus when a write control signal driven on a write control signal line of the bus is asserted during a first stage of an instruction execution pipeline;

if the address is an address of the addressable register, receiving the value via a plurality of data signal lines of the bus when a corresponding ready signal driven on a ready signal line of the peripheral bus is asserted during a second stage of the instruction execution pipeline subsequent to the first stage; and

storing the value in the addressable register.

41 40. A method for modifying a value stored in an addressable register, comprising:

driving an address of the addressable register on a plurality of address signal lines of a bus, an asserted read control signal on a read control signal line of the bus, and an asserted write control signal on a write control signal line of the bus during a first stage of an instruction execution pipeline;

receiving the value via a first plurality of data signal lines of the bus when a corresponding ready signal driven on a ready signal line of the bus is asserted during a second stage of the instruction execution pipeline subsequent to the first stage;

modifying the value during a third stage of the instruction execution pipeline subsequent to the second stage; and

driving the modified value on a second plurality of data signal lines of the bus, and an asserted ready signal on a ready signal line of the bus, during a fourth stage of the instruction execution pipeline subsequent to the third stage.

42 41. The method as recited in claim 40 wherein a time period between the first and second stages of the instruction execution pipeline is extended in the event of a stall condition.

43 42. The method as recited in claim 40 wherein a time period between the third and fourth stages of the instruction execution pipeline is extended in the event of a stall condition.